REMARKS

Claims 1-41 are pending in the application. No claims are presently allowed.

Claims 1, 14, 27, 40, and 41 are amended to clarify that instructions may be dispatched from each thread to the functional unit. Support for this amendment is found at page 10, lines 21-25.

The Office Action is inconsistent as to whether the rejection is non-final or final. It is assumed that the rejection in non-final.

Claim Rejections – 35 U.S.C. § 102

Claims 1-12, 14-26, 28-38, and 41 have been rejected under 35 U.S.C § 102(b) as allegedly anticipated by Motomura (US 5,815,727).

Claim 1 recites an apparatus comprising: a peripheral bus coupled to a peripheral unit and a processing slice coupled to the peripheral bus. The peripheral bus transfers peripheral information including a command message specifying a peripheral operation. The processing slice executes a plurality of threads comprising instructions. The threads include a first thread sending the command message to the peripheral unit. The processing slice comprises a functional unit to perform a register operation specified in the instructions dispatched from each thread. The processing slice executes the instructions from more than one of the plurality of threads concurrently in a clock cycle.

Motomura discloses a multi-thread parallel processor system having a plurality of processors and an ordered multithread executing system (Fig. 1). The ordered multithread executing system determines which thread will execute on each processor.

In order to make a *prima facie* case of anticipation, the reference must disclose each limitation of the claim. *Verdegaal Bros. v. Union Oil Co. of California*, 2 U.S.P.Q.2d 1051, 1053, 814 F.2d 628, 631 (Fed. Cir. 1987); MPEP 2131. Among other deficiencies, the reference does not disclose the limitation in claim 1 that the functional unit performs a register operation specified in the instructions dispatched from each thread.

As amended, claim 1 clarifies that instructions may be dispatched from each thread to the functional unit. This avoids an interpretation that functional unit is capable of executing such instructions, but does not actually do so. In the present claim, instructions may be dispatched from each thread to the functional unit. Thus the functional unit is not dedicated to a single

thread.

The Examiner stated that Fig. 1, structure 100 of Motomura discloses Applicant's processing slice and that Motomura's processor discloses Applicant's functional unit (Office Action of 12/29/2004, p. 3, lines 1-3). Although the system of Motomura as a whole is capable of simultaneous execution of multiple threads, there is no sharing of functional units among threads. Motomura discloses that each processor can execute only one thread at a time, in that the thread must go into a waiting or completed state before another thread is assigned to the processor (col. 8, lines 40-51). Further, there are no connections disclosed between processors. Each processor can communicate only with the ordered multithread execution system and the memory device (Fig. 1). The result of this configuration is that each processor is dedicated only to the one thread that can execute on that processor at a time. An idle processor cannot be allocated to a thread executing on another processor. In the present application, it is specifically recited in the claims that the functional unit can perform a register operation specified in the instructions dispatched from *each* of the threads, which are simultaneously executing. Motomura lacks this capability because each processor can perform operations dispatched from only *one* thread.

Claims 14, 27, and 41 also contain the limitation regarding the functional unit and are asserted to differ from the reference in the same manner as claim 1. Claims 2-12, 15-25, and 28-38 depend from and contain all the limitations of claims 1, 14, or 27 and are also asserted to differ from the reference in the same manner as claim 1.

Claim Rejections – 35 U.S.C. § 103

Claims 13, 26, and 39 have been rejected under 35 U.S.C § 103(a) as allegedly unpatentable over Motomura in view of Hiraoka et al. (US 5,418,917).

Hiraoka discloses a method and apparatus for controlling a conditional branch instruction in a pipeline type data processing apparatus.

In order to make a *prima facie* case of obviousness, each claim limitation must be disclosed in the references (MPEP 2143.03). As in Motomura, Hiraoka does not disclose the limitation in claims 1 (13 dependent thereon), 14 (26 dependent thereon), and 27 (39 dependent thereon) regarding the functional unit. As neither of the references discloses the functional unit, a *prima facie* case of obviousness has not been made.

Claim 40 has been rejected under 35 U.S.C § 103(a) as allegedly unpatentable over Motomura in view of Dove et al. (US 5,938,765).

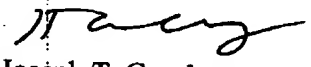
Claim 40 recites a processing system comprising a plurality of multi-thread processors, a plurality of peripheral units, and a peripheral bus. Each processor comprises a plurality of processing slices including a functional unit.

Dove discloses an apparatus and method for initializing a shared-memory, multimode multiprocessor computer system. As in Motomura, Dove does not disclose the limitation in claim 40 regarding the functional unit. As neither of the references discloses the functional unit, a *prima facie* case of obviousness has not been made.

In view of the foregoing, it is submitted that the application is now in condition for allowance.

In the event that a fee is required, please charge the fee to Deposit Account No. 50-0281, and in the event that there is a credit due, please credit Deposit Account No. 50-0281.

Respectfully submitted,



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